

CLAIMS

What is claimed is: 1. An ultrasonic transducer, comprising: 1 an ultrasonic sensor having a plurality of elements; and 2 an integrated circuit formed on a wafer, the wafer including a plurality of cavities 3 defining a plurality of posts such that the cavities alter the acoustic impedance of the 4 wafer, and wherein the integrated circuit is joined to the ultrasonic sensor. 5 The transducer of claim 1, wherein the ultrasonic sensor comprises 2. 1 piezoelectric ceramic material. 2 The transducer of claim 1, wherein the ultrasonic sensor comprises a 1 micro-machined ultrasonic transducer (MUT). 2 4. The transducer of claim 1, wherein each elements of the ultrasonic sensor 1 is located over one of the plarality of posts. 2 The transducer of daim 1, wherein each of the elements of the ultrasonic 5. 1 sensor are located over one of the plurality of cavities. 2

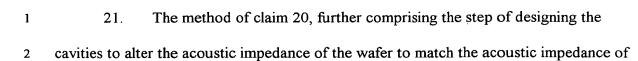
- 1 6. The transducer of claim 1, wherein the cavities reduce acoustic energy
- 2 traveling laterally in the wafer.

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7. The transducer of claim 1, wherein the wafer is silicon.

- 1 8. The transducer of claim 1, wherein the wafer is germanium.
- 1 9. The transducer of claim 1, wherein the cavities are designed to allow the
- 2 acoustic impedance of the wafer to match the acoustic impedance of the transducer
- 3 elements.
- 1 10. The transducer of claim 1, wherein altering the acoustic impedance of the wafer increases the effective bandwidth of the transducer elements.
- 1 The transducer of claim 1, wherein the wafer further comprises:
- a first wafer component including the plurality of cavities; and
- a second wafer component bonded to the first wafer component.
- 1 12. A method for forming an ultrasonic transducer, the method comprising
- 2 the steps of:
- forming a plurality of cavities in a first wafer component such that the cavities
- 4 define the acoustic impedance of the first wafer component and such that the cavities
- 5 define a plurality of posts;
- 6 joining a second wafer component to the first wafer component;
- forming an integrated circuit on a surface of the second wafer component;
- forming an ultrasonic sensor having a plurality of elements; and
- 9 joining the ultrasonic sensor to the integrated circuit.

- 1 13. The method of claim 12, wherein the ultrasonic sensor comprises
- 2 piezoelectric ceramic material.
- 1 14. The method of claim 12, wherein the ultrasonic sensor comprises a
- 2 micro-machined ultrasonic transducer (MUT).
- 1 15. The method of claim 12, further comprising the step of locating each of
- the elements of the ultrasonic sensor over one of the plurality of posts.
- 1 16. The method of claim 12, further comprising the step of locating each of
- the elements of the ultrasonic sensor over one of the plurality of cavities.
- 1 The method of claim 12, wherein the cavities reduce acoustic energy
- 2 traveling laterally in the substrate.
- 1 18. The method of claim 12, wherein the first wafer component and the
- 2 second wafer component are silicon.
- 1 19. The method of claim 12, wherein the first wafer component and the
- 2 second wafer component are germanium.
- 1 20. The method of claim 12, wherein the first wafer component and the
- 2 second wafer component form an acoustically variable wafer.



- 3 the transducer elements.
- The method of claim 20, further comprising the step of altering the acoustic impedance of the wafer to increase the effective bandwidth of the transducer elements.
- 1 23. An acoustically variable wafer, comprising:
- a first wafer component having a plurality of cavities defining a plurality of posts

 such that the cavities alter the acoustic impedance of the first wafer component; and

 a second wafer component bonded to the first wafer component, the first wafer
- component and the second wafer component forming the wafer, where the wafer has a variable acoustic impedance.
- 1 24. The wafer of claim 23, further comprising an integrated circuit formed 2 over a surface of the wafer.
- 1 25. The wafer of claim 23, further comprising a micro-machined ultrasonic 2 transducer formed over a surface of the wafer.
- 1 26. The wafer of claim 23, wherein the wafer comprises a circuit board.